Chaitanya Mamatha Ananda

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Research Interests

My research interests lie in the areas of compiler optimization, machine learning and deep learning. My doctoral research has involved (i) building optimized memory layouts for heap segment in x86 binaries, (ii) devising techniques for reducing code size in x86/Arm binaries and (iii) AI-driven techniques for improving code layout.

Education

2022 – present	Ph.D. Candidate in Computer Science, University of California, Riverside Advisor: Dr. Rajiv Gupta
2017 – 2021	B.E. in Computer Science and Engineering, Bangalore Institute of Technology, Bengaluru, India.

Professional Experience

Sept 2025 – May 2026	**Student Researcher at Google, Sunnyvale** *Exploring AI-driven approaches for improving code layout optimization* *Designing techniques to improve memory layout on warehouse scale workloads*
2023 – 2025 Summer	**Graduate Research Assistant at University of California, Riverside** *Conducted research to improve memory layouts* *Designed techniques to reduce code size in binaries*
2019 – 2022	**Research Intern at Indian Institute of Science, Bengaluru, India** *Developed a parallel programming model for solving partial differential equations using Regent/Legion* *Designed an anomaly detector for scientific data using statistical and neural network based methods*
2021 Spring	**Project Trainee at Robert Bosch Engineering and Business Solutions (RBEI), Bengaluru, India** *Developed scripts to synchronize video and radar data from automated test driving*

Doctoral Research Projects

PreFix	Developed *PreFix*, a novel optimization technique for heap-intensive applications that achieves near-perfect separation of hot objects, improving spatial locality and application performance. *PreFix* employs profiling-guided hot object identification, preallocated memory regions, and object recycling, resulting in an average execution time reduction of 21.7% (up to 74%), significantly outperforming existing solutions like HDS and HALO. [CGO '25]
DeduBB	Developed a framework for reducing the size of production binaries on x86 and Arm architectures at the post-link stage. [LCTES '26]

Technical Skills

Programming	Python, C/C++
Frameworks	LLVM (BOLT)
Tools	Vim, Linux/Unix, Git

Publications

CGO '25 Chaitanya Mamatha Ananda, Rajiv Gupta, Sriraman Tallam, Han Shen and Xinliang David Li. **PreFix: Optimizing the Performance of Heap-Intensive Applications,** *The IEEE/ACM International Conference on Code Generation and Optimization (CGO)*, 2025

LCTES '26 Chaitanya Mamatha Ananda, Mahbod Afarin, Rajiv Gupta, Sriraman Tallam, Han Shen and Xinliang David Li. **DeduBB: Binary Code Size Reduction via Post-Link Basic Block Deduplication,** *ACM SIGPLAN/SIGBED International Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, 2026

Honors and Awards

2022 Dean's Distinguished Fellowship, University of California, Riverside

2011 Inspire Award, Department of Science and Technology, Government of India

Teaching Experience

2025 Summer Compiler Design

2024 Summer Compiler Design

2023 Fall Compiler Construction

Relevant Courses

2024 Winter Artificial Intelligence

2023 Fall Introduction to Deep Learning

2023 Spring Advanced Computer Architecture

2023 Winter Advanced Operating Systems

2022 Fall High Performance Computing

2022 Fall Compiler Construction

Talks

2024 **Google:** Presented technical deep-dive on heap layout optimization strategies (PreFix) to the Compiler Optimization Team.